L Number	Hits	Search Text	DB	Time stamp
1	88544	((transist$4 same circuit) or (memory same circuit)) and (configuration same circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:20
2	4000	(tri-state or (tri adj state) or (three adj state)) and (((transist$4 same circuit) or (memory same circuit)) and (configuration same circuit))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:20
3	2194	((tri-state or (tri adj state) or (three adj state)) and (((transist$4 same circuit) or (memory same circuit)) and (configuration same circuit))) and identif$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:04
4	2099	(((tri-state or (tri adj state) or (three adj state)) and (((transist$4 same circuit) or (memory same circuit)) and (configuration same circuit))) and identif$5) and determin$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:04
5	221	((((tri-state or (tri adj state) or (three adj state)) and (((transist$4 same circuit) or (memory same circuit)) and (configuration same circuit))) and identif$5) and determin$4) and FET and RAM	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:26
6	171	(((((tri-state or (tri adj state) or (three adj state)) and (((transist$4 same circuit) or (memory same circuit)) and (configuration same circuit))) and identif$5) and determin$4) and FET and RAM) and feedback	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:05
7	121	((((((tri-state or (tri adj state) or (three adj state)) and (((transist$4 same circuit) or (memory same circuit)) and (configuration same circuit))) and identif$5) and determin$4) and FET and RAM) and feedback) and node	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:18
8	3	(((((((tri-state or (tri adj state) or (three adj state)) and (((transist$4 same circuit) or (memory same circuit)) and (configuration same circuit))) and identif$5) and determin$4) and FET and RAM) and feedback) and node) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:19
9	215	(tri-state or (tri adj state) or (three adj state)) same (configuration near4 circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:25
10	5	((tri-state or (tri adj state) or (three adj state)) same (configuration near4 circuit)) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:21
11	6	((tri-state or (tri adj state) or (three adj state)) same (configuration near4 circuit)) and FET and RAM	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:21
13	3	(((tri-state or (tri adj state) or (three adj state)) same logic) same (configuration near4 circuit)) and FET and RAM and feedback	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:26

12	63	((tri-state or (tri adj state) or (three adj state)) same logic) same (configuration near4 circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:32
14	26	(((tri-state or (tri adj state) or (three adj state)) same logic) same (configuration near4 circuit)) and node	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/17 19:32

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20030179318 A1	20030925	12	Self-adjusting pixel clock and method therefor	348/537
2	US 20030039141 A1	20030227	20	Data holding circuit having backup function	365/185.11
3	US 20020149968 A1	20021017	17	Data holding circuit having backup function	365/189.05
4	US 20020125912 A1	20020912	11	Tri-state buffer circuit	326/58
5	US 20020070805 A1	20020613	12	Circuit configuration with an integrated amplifier	330/264
6	US 20020057108 A1	20020516	29	Semiconductor integrated circuit	326/104
7	US 6639845 B2	20031028	16	Data holding circuit having backup function	365/189.05
8	US 6563341 B2	20030513	11	Tri-state buffer circuit	326/58
9	US 6559721 B2	20030506	11	Circuit configuration with an integrated amplifier	330/264
10	US 6493272 B1	20021210	18	Data holding circuit having backup function	365/189.05
11	US 6484296 B1	20021119	18	Electrical rules checker system and method for reporting problems with tri-state logic in electrical rules checking	716/5
12	US 6484295 B1	20021119	17	Electrical rules checker system and method providing quality assurance of tri-state logic	716/4
13	US 6476753 B1	20021105	37	Analog to digital converter using magnetoresistive memory technology	341/155
14	US 6314020 B1	20011106	36	Analog functional module using magnetoresistive memory technology	365/158
15	US 6313661 B1	20011106	8	High voltage tolerant I/O buffer	326/81

	Document ID	Issue Date	Pages	Title	Current OR
16	US 6307767 B1	20011023	13	Low power priority encoder	365/49
17	US 6272040 B1	20010807	37	System and method for programming a magnetoresistive memory device	365/158
18	US 6252795 B1	20010626	37	Programmable resistive circuit using magnetoresistive memory technology	365/158
19	US 6252471 B1	20010626	36	Programmable oscillator using magnetoresistive memory technology	331/179
20	US 6225933 B1	20010501	37	Digital to analog converter using magnetoresistive memory technology	341/144
21	US 6188240 B1	20010213	137	Programmable function block	326/39
22	US 6150807 A	20001121	7	Integrated circuit architecture having an array of test cells providing full controllability for automatic circuit verification	324/158.1

	Document ID	Issue Date	Pages	Title	Current OR
23	US 6064244 A	20000516	25	Phase-locked loop circuit permitting reduction of circuit size	327/158
24	US 6006327 A	19991221	7	Option setting device and method for providing various settings through software means to a computer motherboard	713/1
25	US 5880617 A	19990309	19	Level conversion circuit and semiconductor integrated circuit	327/333
26	US 5880613 A	19990309	18	Logic storing circuit and logic circuit	327/202
27	US 5872448 A	19990216	9	Integrated circuit architecture having an array of test cells providing full controlability for automatic circuit verification	324/158.1
28	US 5804985 A	19980908	10	Programmable output buffer and method for programming	326/39
29	US 5726587 A	19980310	12	BiCMOS tri-state buffer with low leakage current	326/56
30	US 5623221 A	19970422	23	Low noise MOSFET employing selective drive signals	327/108
31	US 5592104 A	19970107	8	Output buffer having transmission gate and isolated supply terminals	326/27
32	US 5555209 A	19960910	14	Circuit for latching data signals from DRAM memory	365/189.05

	Document ID	Issue Date	Pages	Title	Current OR
33	US 5553306 A	19960903	10	Method and apparatus for controlling parallel port drivers in a data processing system	710/8
34	US 5503036 A	19960402	16	Obstruction detection circuit for sample probe	73/864.34
35	US 5498980 A	19960312	7	Ternary/binary converter circuit	326/60
36	US 5446399 A	19950829	5	Method and structure for a fault-free input configuration control mechanism	326/16
37	US 5369646 A	19941129	25	Semiconductor integrated circuit device having test circuit	714/733
38	US 5346318 A	19940913	23	Thermal recording head driving device	400/120.15
39	US 5317211 A	19940531	8	Programmable pin for use in programmable logic devices	326/39
40	US 5175728 A	19921229	15	Flexible interface system for interfacing different complements of port circuits for a PCM telephony switching system	370/359
41	US 5047669 A	19910910	30	Tristate circuit using bipolar transistor and CMOS transistor	326/58
42	US 5027012 A	19910625	18	Programmable logic circuit using wired-or tristate gates	326/114
43	US 4835549 A	19890530	15	Printing head system	347/237
44	US 4833349 A	19890523	14	Programmable logic and driver circuits	326/50
45	US 4803661 A	19890207	11	Low power eprom logic cell and logic arrays thereof	365/184
46	US 4791602 A	19881213	15	Soft programmable logic array	326/38

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47	US 4601053 A	19860715	26	Automatic TV ranging system	382/106
48	US 4573168 A	19860225	13	Balanced bidirectional or party line transceiver accommodating common-mode offset voltage	375/257
49	US 4571588 A	19860218	7	Scaling circuit for remote measurement system	340/870.13
50	US 4529894 A	19850716	7	Means for enhancing logic circuit performance	326/19
51	US 4459693 A	19840710	13	Method of and apparatus for the automatic diagnosis of the failure of electrical devices connected to common bus nodes and the like	714/734
52	US 4081695 A	19780328	5	Base drive boost circuit for improved fall time in bipolar transistor logic circuits	326/56
53	US 4020361 A	19770426	9	Switching mode power controller of large dynamic range	307/106
54	US 3986045 A	19761012	10	High speed logic level converter	326/78
55	US 3912947 A	19751014	7	MOS data bus control circuitry	326/57
56	JP 05143668 A	19930611	8	LOGIC CIRCUIT SIMULATING METHOD	
57	NN9408275	19940801	NA	Fully Tri-Stable On-Chip-Drive and On-Chip-Receiver with Active Termination	
58	NN9408267	19940801	NA	Method to Extend Personal Computer System Memory	

	Document ID	Issue Date	Pages	Title	Current OR
59	NN9204397	19920401	2	Circuit Scheme to Bias OCD Output Stage N-Well.	
60	US 6484295 B	20021119	17	Tri-state logic appraising method of integrated circuit, involves identifying selected circuit configuration and probable circuit configuration at node of integrated circuit	
61	US 6484296 B	20021119	18	Tri-state logic conditions report method for integrated circuit device, involves appraising tri-state elements identified to be equal to selected identification objective circuit configuration	
62	US 5986467 A	19991116	8	Configurable logic modification circuit for time multiplexing programmable logic devices	
63	EP 384429 A	19900829	18	General-purpose small-scale integrated programmable logic circuit - has three-state circuits in wired OR configuration for deriving outputs of gates and combinational logic circuits	